Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Currently amended) A method ~~for validating performance and functionality of a processor,~~ comprising the steps of:

executing a program on a high level simulator of ~~said~~ a processor; thereafter

dividing the program into a plurality of independent code fragments such that a destination branch of an instruction in each code fragment falls within that code fragment; thereafter

establishing a plurality of checkpoints; wherein each of the plurality of checkpoints is established along one of a beginning point or an ending point of a different one of the code fragments; thereafter

saving state data at each of said checkpoints; ~~and~~ thereafter

executing instructions in ~~running~~ said program on a plurality of low level simulators of said processor in parallel, starting each of said low level simulators at a corresponding checkpoint with corresponding state data associated with said corresponding checkpoint, and thereafter

generating functional data to validate functionality of the processor.

2. (Currently amended) The method of claim 1 ~~wherein said checkpoints divide said program into code fragments of determined lengths~~ further comprising:

generating performance data to validate performance of the processor.

3. (Currently amended) The method of claim 1 wherein ~~said checkpoints divide said program into~~ each code fragments has one of random lengths and determined length.

4. (Previously presented) The method of claim 1 wherein said state data comprises:

program counter contents of said processor;

register contents of said processor;

cache memory contents of said processor;

main memory contents of said processor; and

branch prediction contents of said processor.

5. (Original) The method of claim 1 wherein said processor is one of (a) a microprocessor, (b) a digital signal processor, (c) an input/output (I/O) controller, and (d) a network processor.

6. (Original) The method of claim 1 wherein said high level simulator is one of (a) an instruction accurate simulator (IAS) of said processor and (b) a cycle accurate simulator (CAS) of said processor.

7. (Original) The method of claim 1 wherein each of said low level simulators is a register transfer level (RTL) model of said processor, written as one of (a) a VHDL model of said processor and (b) a Verilog model of said processor.

8. (Original) The method of claim 1 wherein said running step further comprises the steps of:

loading each of said low level simulators with said program;

initializing each of said low level simulators at said corresponding checkpoint with said corresponding state data associated with said corresponding checkpoint; and

executing said program on said low level simulator up to a certain point in said program.

9. (Original) The method of claim 8 wherein said certain point is one of (a) a next checkpoint immediately following said corresponding checkpoint, (b) a point in said program a random length after said corresponding checkpoint, and (c) a point after said corresponding checkpoint.

10. (Original) The method of claim 1 wherein said running step further comprises generating one of (a) functional data of said processor and (b) performance data of said processor.

11. (Currently amended) A computer readable media having stored thereon a program ~~for validation of performance and functionality of a processor,~~ comprising computer readable instructions for:

executing a program on a high level simulator of ~~said~~ a processor; thereafter

dividing the program into a plurality of independent code fragments such that a destination branch of an instruction in each code fragment falls within that code fragment; thereafter

establishing a plurality of checkpoints; wherein each of the plurality of checkpoints is established along one of a beginning point or an ending point of a different one of the code fragments; thereafter

saving state data at each of said checkpoints; ~~and~~ thereafter

executing instructions in ~~running~~ said program on a plurality of low level simulators of said processor in parallel, starting each of said low level simulators at a corresponding checkpoint with corresponding state data associated with said corresponding checkpoint, and thereafter

generating functional data to validate functionality of the processor.

12. (Currently amended) The computer readable media of claim 11 ~~wherein said checkpoints divide said program into code fragments of determined lengths~~ further comprising:

generating performance data to validate performance of the processor.

13. (Currently amended) The computer readable media of claim 11 wherein ~~said checkpoints divide said program into~~ each code fragment~~s~~ has one of random length~~s~~ and determined length

14. (Original) The computer readable media of claim 11 wherein said computer readable instructions for running said program on a plurality of low level simulators of said processor in parallel, further comprises computer readable instructions for:

loading each of said low level simulators with said program;

initializing each of said low level simulators at said corresponding checkpoint with said corresponding state data associated with said corresponding checkpoint; and

executing said program on said low level simulator up to a certain point in said program.

15. Canceled.